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10670883  
corrected

SPECIFICATION

BLOCK SYMMETRIZATION IN A FIELD PROGRAMMABLE  
GATE ARRAY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of co-pending United States Patent  
Application Serial Number 09/880,629, filed June 12, 2001, which is a  
continuation of United States Patent Application Serial Number 09/518,974, filed  
March 6, 2000, now issued as United States Patent Number 6,268,743.  
*is now a U.S. Patent 6,680,624*

BACKGROUND OF THE INVENTION

1. Field Of The Invention

[0002] The present invention relates to a field programmable gate array  
(FPGA) architecture.

[0003] More particularly, the present invention relates to structures for  
coupling routing resources to one another in an FPGA architecture.